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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/067,372	WANG ET AL.	
	Examin r	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *76-134* is/are pending in the application.

4a) Of the above claim(s) *107-134* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *76-106* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Pri rity under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20050111*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 76-106, drawn to A method for providing ordered capture clocks to detect or locate faults within N clock domains comprising the steps of compacting N output responses of all said scan cells to signatures during the compact operation, classified in class 714, subclass 732.

   II. Claims 107-109 and 132-134, drawn to A method for providing ordered capture clocks to detect or locate faults within N clock domains comprising the step of shifting-out N output responses of all said scan cells for analysis during a shift-out operation, classified in class 714, subclass 726.

   III. Claims 110-131, drawn to A method for providing ordered capture clocks to detect or locate faults within N clock domains comprising the step of comparing N output responses directly with their expected output responses for all said scan cells within said N clock domains and indicating errors immediately during a compare operation, classified in class 714, subclass 736.

The inventions are distinct, each from the other because of the following reasons: Inventions Groups I, II and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if

they are shown to be separately usable. In the instant case, invention Group I has separate utility such as for a method comprising the steps of compacting N output responses of all said scan cells to signatures during the compact operation. In the instant case, invention Group II has separate utility such as for a method comprising the step of shifting-out N output responses of all said scan cells for analysis during a shift-out operation. In the instant case, invention Group III has separate utility such as for a method comprising the step of comparing N output responses directly with their expected output responses for all said scan cells within said N clock domains and indicating errors immediately during a compare operation. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Groups I, II and III are mutually exclusive, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Jim Zeeger on 1/10/2005 a provisional election was made without traverse to prosecute the invention of Group I, claims 76-106. Affirmation of this election must be made by applicant in replying to this Office action. Claims 107-134 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

This application contains claims 107-134 drawn to an invention nonelected without traverse on 1/10/2005. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Drawings

2. The drawings were received on 02/07/2002. These drawings are accepted.

Response to Arguments

3. Applicant's arguments with respect to claims 76-106 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 76-106 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Claim 76 recites new matter, "(b) applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least two said capture clock pulses from two or more selected capture clocks placed in a sequential order, wherein each said selected capture clock must contain at least one said capture clock pulse **and does not contain any said shift clock pulse**" [Emphasis Added]. The limitation "each said selected capture clock must contain at least one said capture clock pulse **and does not contain any said shift clock pulse**" [Emphasis Added] critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). The Examiner asserts that any clock is comprised of only pulses belonging to the particular clock and cannot be comprised of pulses belonging to any other clock. Hence a capture clock is comprised of only pulses belonging to the capture clock, i.e., capture clock pulses, and cannot be comprised of shift clock pulses because shift clock pulses belong to a shift clock not a capture clock. The Examiner would like to point out that the Examiner does not believe that is what the Applicant intends anyway. On page 10,

lines 4-16 of the applicant's specification the Applicant teaches that a capture cycle does not contain any shift pulses.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 76-106 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 76 recites new matter, "(b) applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least two said capture clock pulses from two or more selected capture clocks placed in a sequential order, wherein each said selected capture clock must contain at least one said capture clock pulse **and does not contain any said shift clock pulse**" [Emphasis Added]. The Examiner asserts that any clock is comprised of only pulses belonging to the particular clock and cannot be comprised of pulses belonging to any other clock. Hence a capture clock is comprised of only pulses belonging to the capture clock, i.e., capture clock pulses, and cannot be comprised of shift clock pulses because shift clock pulses belong to a shift clock not a capture clock. The Examiner would like to point out that the Examiner does not believe that is what the Applicant intends anyway. On page 10, lines 4-16 of the applicant's specification the Applicant teaches that a capture cycle does not contain any shift pulses.

Claims 76-106 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claim 76 recites new matter, "(b) applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least two said capture clock pulses from two or more selected capture clocks placed in a sequential order, wherein each said selected capture clock must contain at least one said capture clock pulse **and does not contain any said shift clock pulse**" [Emphasis Added]. The omitted structural cooperative relationships are: The relationship between a "capture clock", a "shift clock", a "capture clock pulse" and a "shift clock pulse".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 76-79, 81, 85-95, 102, 105 and 106 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie; Benoit et al. (US 6442722 B1, hereafter referred to as Nadeau-Dostie1) in view of Nadeau-Dostie; Benoit et al. (US 5349587 A, hereafter referred to as Nadeau-Dostie2).

35 U.S.C. 103(a) rejection of claims 76, 105 and 106.

Nadeau-Dostie1 teaches a method for providing capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in self-test mode, where N>1 and each domain has a plurality of scan cells (see Abstract in Nadeau-Dostie1), said method comprising the steps of: a. generating and loading N pseudorandom stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during the shift operation (col. 24, lines 7-10 in Nadeau-Dostie1 teaches generating and loading N pseudorandom stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during the shift operation); b. applying a sequence of capture clocks to all said scan cells within said N clock domains during the capture operation (col.8, lines 16-21 in Nadeau-Dostie1 teaches that the domain clocks are use to perform the capture operation: Note; ClockHS in Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 is a capture clock); c. compacting N output responses of all said scan cells to signatures during the compact operation (see col. 7, lines 46-52 in Nadeau-Dostie1; Note: and MISR is a device for compacting N output responses of all said scan cells to

signatures during the compact operation); and d. repeating the steps of a-c until a predetermined limiting criteria is reached, wherein steps a and c occur substantially concurrently (col.8, lines 16-21 in Nadeau-Dostie1 teaches that the domain clocks are use to perform the capture operation and launch the last bit of the test stimuli, hence steps a and c occur substantially concurrently; Note: col. 8, lines 12-16 in Nadeau-Dostie1 teaches that, prior to performing the capture operation and launch the last bit of the test stimuli, shifting in the test stimulus is performed concurrently with the capture operation: Note also signature analysis is a means for preparing output responses for signature analysis). In addition, claim 76 recites new matter, "(b) applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least two said capture clock pulses from two or more selected capture clocks placed in a sequential order, wherein each said selected capture clock must contain at least one said capture clock pulse **and does not contain any said shift clock pulse**" [Emphasis Added]. The Examiner asserts that any clock is comprised of only pulses belonging to the particular clock and cannot be comprised of pulses belonging to any other clock. Hence a capture clock is comprised of only pulses belonging to the capture clock, i.e., capture clock pulses, and cannot be comprised of shift clock pulses because shift clock pulses belong to a shift clock not a capture clock.

However Nadeau-Dostie1 does not explicitly teach the specific use of an ordered capture clocks.

Nadeau-Dostie2, in an analogous art, teaches an ordered sequence of clock signals (ck1, ck2 and ck3 in Figure 4 of Nadeau-Dostie2). The Examiner would like to point out that clocks from different clock domains require a means for identifying the clocks and associating them with their respective clock domains. Creating an ordered sequence of labels to identify the clocks and respective clock domains is a common way of identifying clock signals.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nadeau-Dostie1 with the teachings of Nadeau-Dostie2 by including use of an ordered capture clocks. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an ordered capture clocks would have provided the opportunity for identifying the clocks and associating them with their respective clock domains.

35 U.S.C. 103(a) rejection of claim 77.

Nadeau-Dostie1 and Nadeau-Dostie2 teach that each said capture clock is programmable to contain one or more clock pulses for performing said shift/compact and capture operations on all said scan cells within one said clock domain (Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 is a programmable device containing clock pulses BistCLK and ClockHS-raw for performing said shift/compact and capture operations on all said scan cells within one said clock domain); wherein said clock domain is solely controlled by said capture clock (Auxiliary Controller 52 in Figures

1 and 2 in Nadeau-Dostie1 uses capture clock ClockHS to control all clock domain operations during testing); and said capture clock can be either generated internally or controlled externally (the capture clock ClockHS in Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 can either generated internally or controlled externally depending on whether BistCLK and ClockHS-raw are internal or external signals), and can operate either at its rated clock speed (at-speed) or at a selected clock speed (ClockHS in Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 can operate either at its rated clock speed ClockHS-raw or at a selected clock speed BistCLK).

35 U.S.C. 103(a) rejection of claim 78.

Nadeau-Dostie1 and Nadeau-Dostie2 teach providing N scan enable signals each within one said clock domain (SEHS in Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1); wherein said SE signals are used to switch operations from shift/compact to capture, and vice versa; and further said SE signals can be generated internally or controlled externally, and are operated either at the rated clock speeds (at-speed) or at selected clock speeds (see Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1).

35 U.S.C. 103(a) rejection of claim 79.

Nadeau-Dostie1 and Nadeau-Dostie2 teach said providing N scan enable (SE) signals further comprises using one global scan enable (GSE) signal to drive said N scan enable (SE) signals; wherein said GSE signal is operated at a selected reduced clock

speed (SE[2] in Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 is a global scan enable signal).

35 U.S.C. 103(a) rejection of claims 81 and 102.

Nadeau-Dostie1 and Nadeau-Dostie2 teach the step of comparing said signatures with their expected signatures for error indication, after said predetermined limiting criteria is reached; wherein said step of comparing said signatures with their expected signatures further comprises comparing said signatures inside said integrated circuit or circuit assembly or shifting out said signatures for comparison in an ATE (col. 9, lines 25-28 in Nadeau-Dostie2).

35 U.S.C. 103(a) rejection of claim 85.

Nadeau-Dostie1 and Nadeau-Dostie2 teach performing said capture operation concurrently on a plurality of clock domains which do not have any logic block crossing each other (col 17, lines 23-35 in Nadeau-Dostie1).

35 U.S.C. 103(a) rejection of claims 86, 88 and 89.

Nadeau-Dostie1 and Nadeau-Dostie2 teach the use of capture disable signals CD[0] and CD[1] in Figures 5 and 6, which allow for applying said capture clocks in a selected order for detecting or locating additional faults in said integrated circuit or circuit assembly.

35 U.S.C. 103(a) rejection of claim 87.

Nadeau-Dostie1 and Nadeau-Dostie2 teach various clocks operating at different speeds, i.e., longer or shorter periods.

35 U.S.C. 103(a) rejection of claims 90-95.

Nadeau-Dostie1 and Nadeau-Dostie2 teach selectively operating said capture clock at its rated clock speed for detecting or locating delay faults within the clock domain controlled by said capture clock (Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 is a programmable device containing clock pulses BistCLK and ClockHS-raw for performing said shift/compact and capture operations on all said scan cells within one said clock domain).

5. Claim 80 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie; Benoit et al. (US 6442722 B1, hereafter referred to as Nadeau-Dostie1) and Nadeau-Dostie; Benoit et al. (US 5349587 A, hereafter referred to as Nadeau-Dostie2) in view of Nadeau-Dostie; Benoit et al. (US 6327684 B1, hereafter referred to as Nadeau-Dostie3).

35 U.S.C. 103(a) rejection of claim 80.

Nadeau-Dostie1 and Nadeau-Dostie2 substantially teaches the claimed invention described in claims 76-79 (as rejected above). In addition, Nadeau-Dostie1 and Nadeau-Dostie2 teach that each said capture clock is programmable to contain one or

more clock pulses for performing said shift/compact and capture operations on all said scan cells within one said clock domain (Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 is a programmable device containing clock pulses BistCLK and ClockHS-raw for performing said shift/compact and capture operations on all said scan cells within one said clock domain); wherein said clock domain is solely controlled by said capture clock (Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 uses capture clock ClockHS to control all clock domain operations during testing); and said capture clock can be either generated internally or controlled externally (the capture clock ClockHS in Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 can either generated internally or controlled externally depending on whether BistCLK and ClockHS-raw are internal or external signals), and can operate either at its rated clock speed (at-speed) or at a selected clock speed (ClockHS in Auxiliary Controller 52 in Figures 1 and 2 in Nadeau-Dostie1 can operate either at its rated clock speed ClockHS-raw or at a selected clock speed BistCLK).

However Nadeau-Dostie1 and Nadeau-Dostie2 do not explicitly teach the specific use of skewing capture clocks so that at any given time only scan cells within one said clock domain are changing states to reduce power consumption.

Nadeau-Dostie3, in an analogous art, teaches the specific use of skewing capture clocks so that at any given time only scan cells within one said clock domain are changing states to reduce power consumption (col. 8, lines 12-19, Nadeau-Dostie3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nadeau-Dostie1 and Nadeau-Dostie2 with the teachings

of Nadeau-Dostie3 by including the specific use of skewing capture clocks so that at any given time only scan cells within one said clock domain are changing states to reduce power consumption. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the specific use of skewing capture clocks so that at any given time only scan cells within one said clock domain are changing states to reduce power consumption would have provided the opportunity to reduce power consumption.

6. Claims 82-84, 96-101, 103 and 104 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie; Benoit et al. (US 6442722 B1, hereafter referred to as Nadeau-Dostie1) and Nadeau-Dostie; Benoit et al. (US 5349587 A, hereafter referred to as Nadeau-Dostie2) in view of Rajski; Janusz et al. (US 5991909 A, hereafter referred to as Rajski).

35 U.S.C. 103(a) rejection of claims 82 and 96.

Nadeau-Dostie1 and Nadeau-Dostie2 substantially teaches the claimed invention described in claims 1-6 (as rejected above).

However Nadeau-Dostie1 and Nadeau-Dostie2 do not explicitly teach the specific use of a plurality of PRPGs.

Rajski, in an analogous art, teaches use of a plurality of PRPGs (see Figure 6 in Rajski). Note also that each of the LFSR PRPG circuits in Figures 1 and 6 are connected to Combinational Phase Shifter logic between the LFSRs and the scan chains. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nadeau-Dostie1 and Nadeau-Dostie2 with the teachings of Rajski by including use of a plurality of PRPGs. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a plurality of PRPGs would have provided the opportunity to provide different and independent sets of pseudorandom test stimuli to different functional logic units.

35 U.S.C. 103(a) rejection of claim 83.

Nadeau-Dostie1, Nadeau-Dostie2 and Rajski teach a finite-state machine to automatically generate a number of test patterns; wherein said test patterns are applied through a phase shifter to a plurality of clock domains (see Figure 6 in Rajski; Note: an LFSR is a finite-state machine to automatically generate a number of test patterns).

35 U.S.C. 103(a) rejection of claim 84.

LFSR PRPG circuits in Figures 1 and 6 are connected to Combinational Phase Shifter logic between the LFSRs and the scan chains to decompress test patterns.

35 U.S.C. 103(a) rejection of claims 97-101, 103 and 104.

Nadeau-Dostie1, Nadeau-Dostie2 and Rajski substantially teaches the claimed invention described in claims 1-20 (as rejected above).

However Nadeau-Dostie1, Nadeau-Dostie2 and Rajski do not explicitly teach the specific use of combinational logic.

The Examiner asserts that use of specific hardware component does not deviate from the scope or the intent of the teachings in the Nadeau-Dostie1, Nadeau-Dostie2 and Rajski patents since one of ordinary skill in the art at the time the invention was made would have known how to design the components in the Nadeau-Dostie1, Nadeau-Dostie2 and Rajski patents using common combinational logic base on design requirements for proper operation and obvious engineering design choices given the design requirements.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Nadeau-Dostie1, Nadeau-Dostie2 and Rajski by including use of combinational logic. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that usé of combinational logic would have provided the opportunity to implement the design taught in the Nadeau-Dostie1, Nadeau-Dostie2 and Rajski patents using common combinational logic base on design requirements and obvious engineering design choices given the design requirements.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133